New Tools for Analysis and Debug of Embedded Core Processors

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Innovating the HP Way

Real-Time Trace Analysis for Embedded Core Processors

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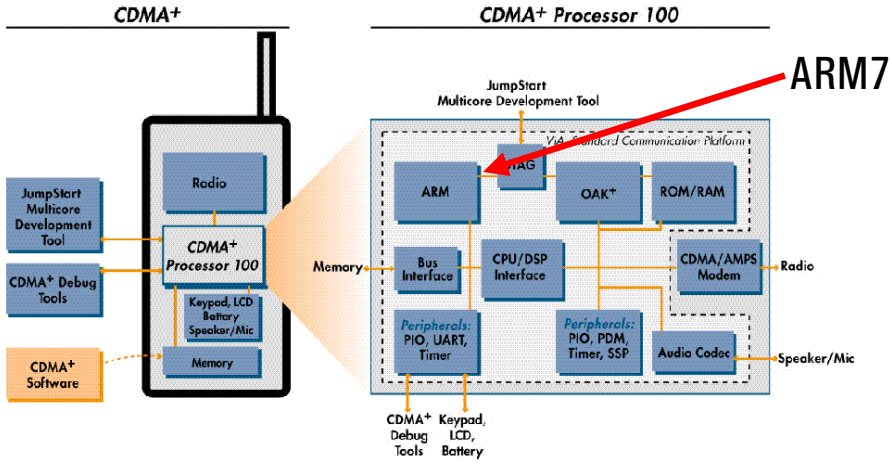
Just as on-chip debugging has provided the breakthrough needed to accomplish run control on RISC and embedded core processors, on-chip trace opens the way for real-time trace of these devices. In this session we will look at this new technology and the implications for the next generation of highly integrated embedded design projects.

Let's talk about embedded core processors

- There's one in your future
- How to debug it?
  - Access to buses
  - Caches and pipelines

The economics of embedded design and the increasing pressure to deliver smaller, more portable products that offer extended battery life at low cost are forcing design teams to consider embedded core processors. Many projects have already moved most all of the electronics to an ASIC with an embedded core processor. In these systems , all of the processing occurs internal to the ASIC device with only I/O information appearing at the pins.

VLSI Tech CDMA Platform SOC



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Here we see a typical example of a widely used product that is made possible by integrating the electronics into ASICs. This slide shows the architecture of VLSI Technologies ASSP for CDMA handsets. Note an ARM7, an OakDSPCore and other user circuits. The overall architecture of W-CDMA chips will be similar.

Much of the digital value added from the handset designer's value added comes by "programming" the hardware operation of the ASSP through software. This happens in 2 ways. First, the operation of certain functions (for instance the tap weights for filter constants) is programmable through the software. Second, the specific algorithm performed by the MPU and DSP are set by the software.

While the software/hardware integration problem is getting lots of help from co-design tools, experience shows that some of the hardest problems are not found until a prototype system is put into operation.

The industry is currently in the phase where first generation platform chips for W-CDMA are being developed. Most handset users will use on of these chips (ASSP's) in their handset designs

The Debugging Dilemma:

New processors require new solutions for debugging and analysis

- Accelerating development schedules
- Complex processors
- Exponential SW growth
- Complex development environment
- Inadequate tools that are difficult to use

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System on Silicon Designs typically include:

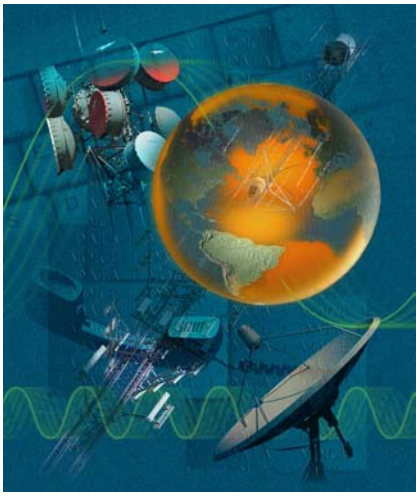
- Embedded Processing Core
- RAM and/or FLASH
- I/O Devices
- DSP Core

Since much of the system is now embedded, a whole new set of problems have been created for the design team that is trying to debug the product and get it completed on time. The team must now deal with :

- Accelerating Development schedules
- Complex processors
- Exponential SW growth
- Complex development environment
- Inadequate tools that are difficult to use

In the next few minutes you'll see:

- Solutions to your most difficult embedded development problems.
- The latest innovations in measurement technology.



In this discussion we will look at some innovative new solutions to the difficult debugging and analysis problems created by the new generation of highly integrated systems-on-silicon embedded systems.

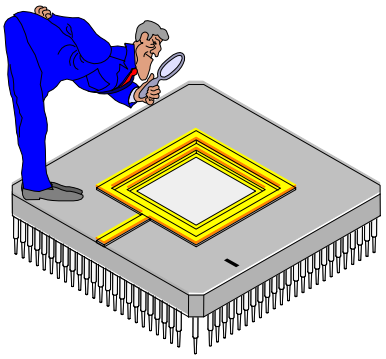
We'll look at New Innovations:

- New technology for real-time trace in embedded core processors.
- New technology for real-time cache-on trace.
- At last! An innovative solution to logic analyzer triggering.

We'll discuss new tools and techniques that provide real-time analysis of processor activity and program execution as it occurs in cache and in deeply embedded cores. We'll see how this data can be presented in various formats including correlated source code. We'll also look at new graphical triggering interface that make s it much easier to perform necessary measurements on complex systems.

The Ideal Probe

- **Designers needs to see:**
  - What's happening on chip pins
  - What's happening inside the chip
- **Static + Dynamic debug**



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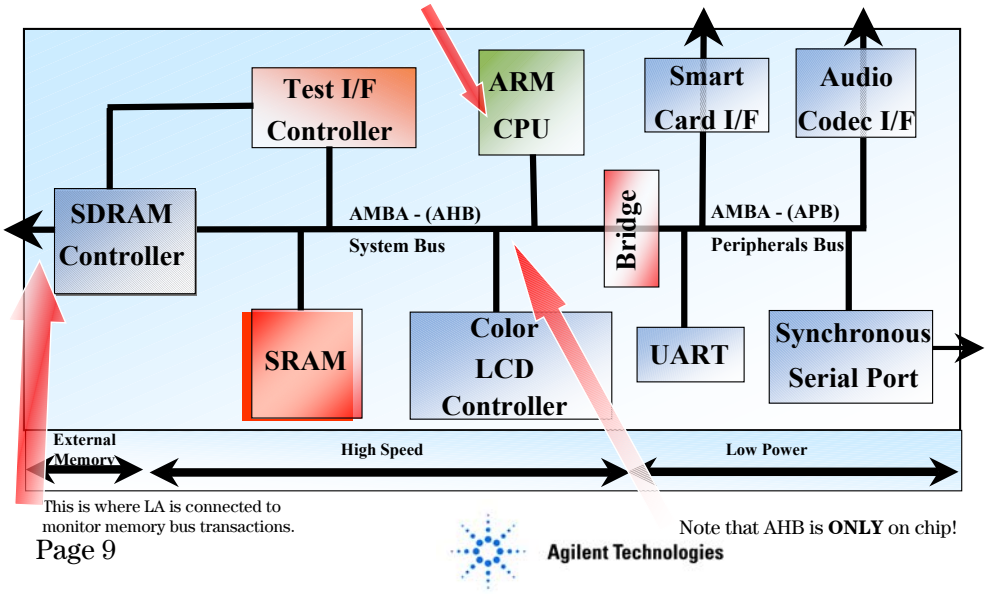
Analysis at the Core

To deal with the need for real-time analysis for embedded core processors, a special analysis version of the device may be developed that has the buses bonded out. Once the design has been debugged, a production version without the pins replaces the analysis version. This approach however, adds both time and cost to the project and makes no provision for analysis on the finished product.

What we need here is a probe that can connect to the inner buses of the core processor and report the activity that occurs there. Since that ideal non-intrusive probe with access to internal buses and registers still doesn't exist, how then can we learn or deduce what takes place deep within and embedded core?

ARM9 and AMBA AHB

N-Trace connects inside here



This is where LA is connected to monitor memory bus transactions.

Note that AHB is **ONLY** on chip!

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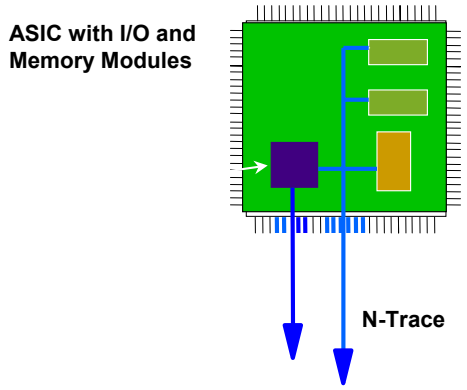
On-Chip Trace Technology



- **Processor**
- **JTAG Control Port**
- **N-Trace Port**

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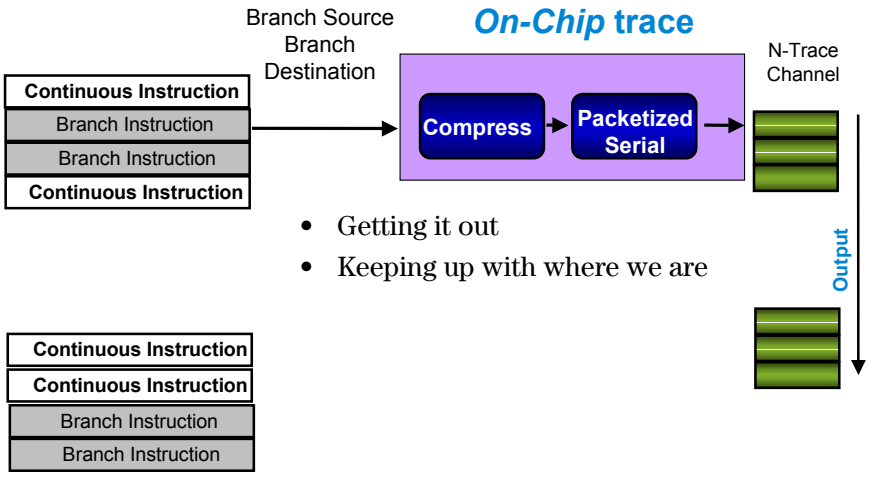
As microprocessors and microcontrollers became more complex, silicon vendors began to add boundry scan circuits into their devices to provide access to registers and control circuits for testing. Tool vendors then began to take advantage of these circuits to gain access into the chip for run control and register display and modification.

Later, some silicon vendors began to enhance the circuits with internal debug monitors and circuits that reported program branch information so that analyzers could reconstruct program execution that occurred in cache.

Now as processor cores are becoming deepluy embedded into ASICs to create systems-on-silicon, vendors are beginning to offer additional circuits that collect essential information about internal program and data. This information is compressed and reported out on to a special trace port.

Moving Data Out of the Core



- Getting it out
- Keeping up with where we are

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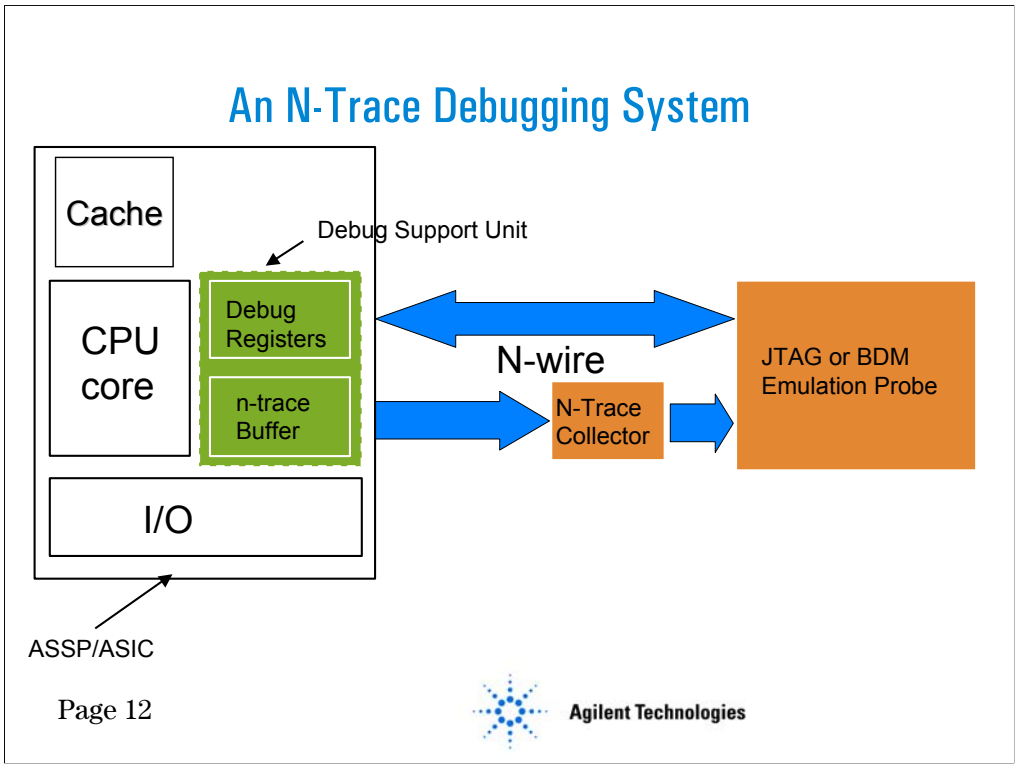
Just as on-chip debugging has provided the breakthrough needed to accomplish run control on RISC and embedded core processors, on-chip trace opens the way for real-time trace of these devices. Information about program branches is collected at the core clock rate , compressed and packetized so that it can be sent out on a small port with just a few pins. An external probe collects the data, decompresses it. This data can then be post processed and correlated to the symbol file generated by the compiler to allow reconstruction of the program execution that took place within the core. Some on-chip trace circuits also provide for the collection of selected data bus information.



Information can be collected using and Emuation Probe and an N-Trace Collector. The On-Chip Embedded Trace Module and Emulation probe work together to form a complete debugging system.

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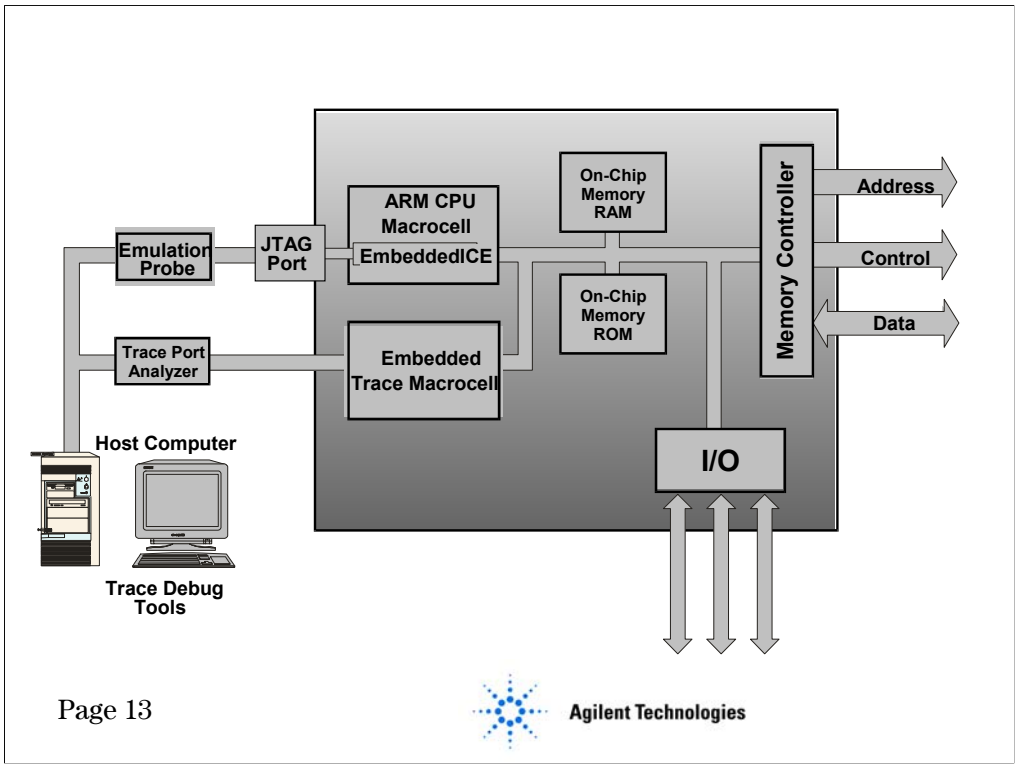
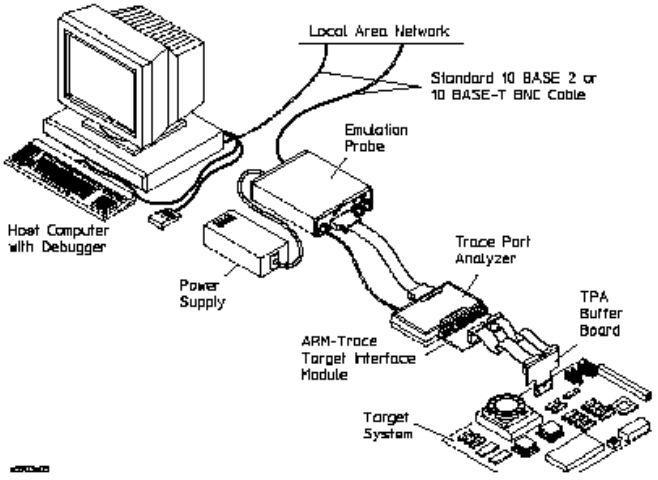


On-chip trace technology allows us to bring a low cost tool to the SW user that is real time, non intrusive and which shows the information needed to trace program behavior.

It integrates very well with debuggers from leading software tool vendors. A debugger is required for the inverse assembly functions, data decompression, and source code referencing on Agilent products. All these functions are performed in the debugger.

TPA Connections



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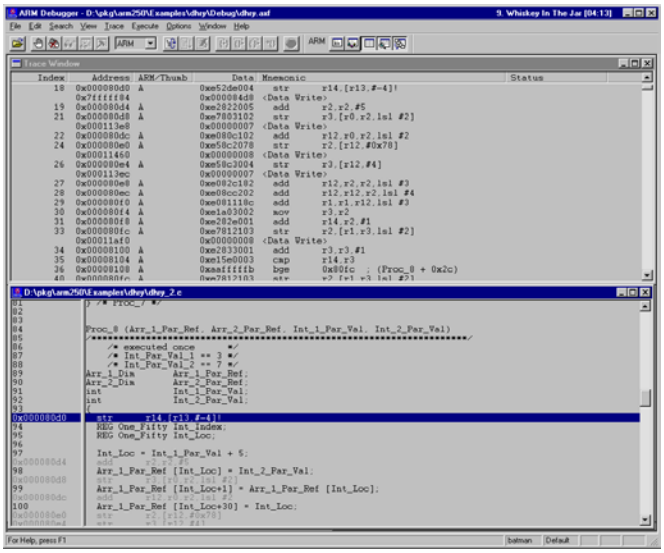
Trace Port Analyzer Display



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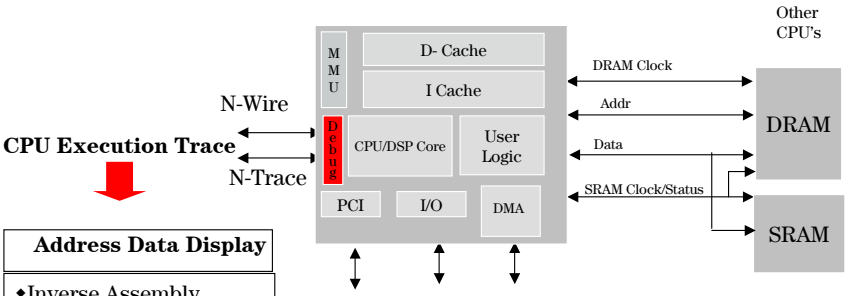
This display shows how the trace data from the ARM Embedded Trace Module captured by the Agilent Trace Port Analyzer is displayed by the ARM Debugger for Windows ADW.

Notice the Inverse Assembly, and Source Code displays.

The System Level Integration Measurement Challenge



Address Data Display

- Inverse Assembly
- Source Code Reference
- Complex Triggering
- Cross Trig
- Cross Sync Data Display

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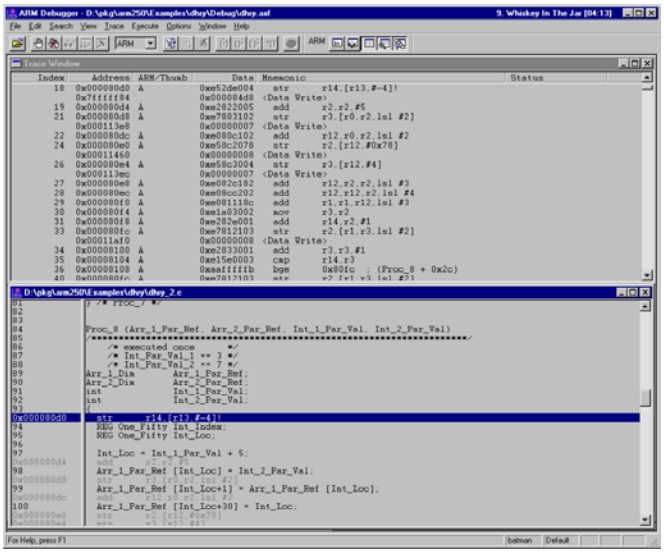
Trace Port Analyzer Display



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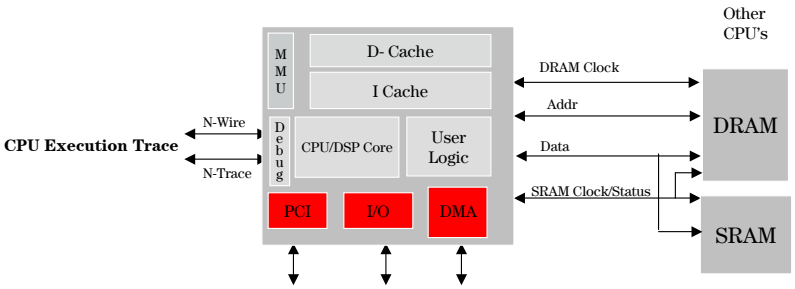

Address/Id DataPacket Status Display

- Bus Cycle Labeling
- Complex Triggering
- Cross Trigger
- Cross Sync Data Display

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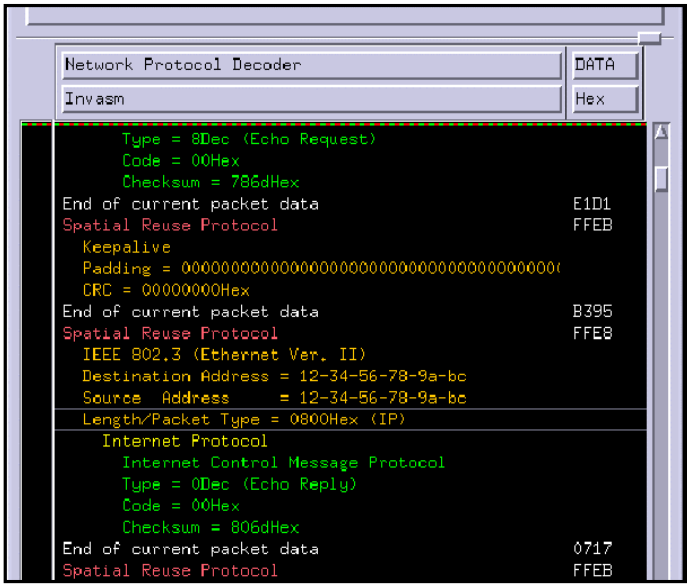

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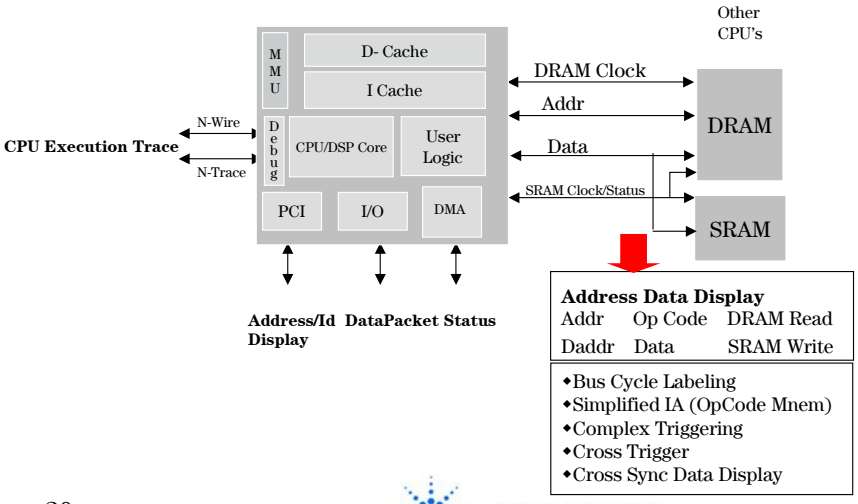

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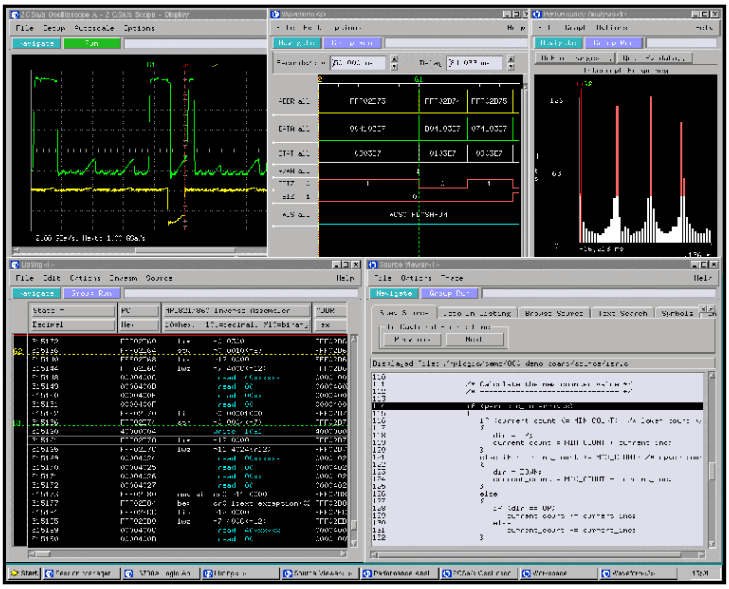

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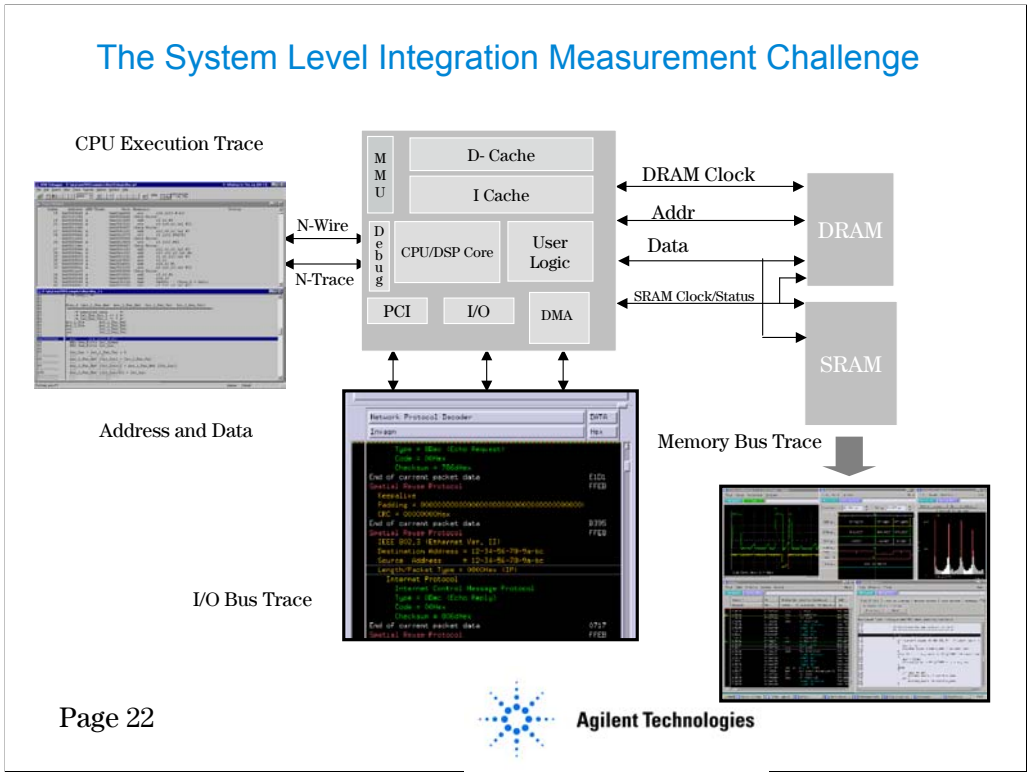

ARM for example, gives the system designer several choices in implementing the Embedded Trace Module. The trace port sends 3 bits of status information and a choice of 4, 8 or 16 bits of trace data. Obviously the wider ports provide greater bandwidth. A use whose programs branch often or who wants to trace many loads and stores will want to use the higher bandwidth (wider) port implementation.

The Agilent Technologies Trace Port Analyzer for ARM supports the 9 and 13 bit wide ports. It works in conjunction with the Agilent Run Control probe and a 3rd party debugger to form a unit. The Trace Port analyzer can capture data up to about 120 MHz

Trace Port Analyzer Solution For Real Time Execution Trace (ARM7,9 ETM)

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Real-time analysis of program and data within the core can be added to the measurement system with the addition of a trace port analyzer.

Here we can see the realization of a trace port collector from Agilent Technologies. This one is designed for the ARM Trace Port now available on selected ARM 7 and ARM 9 core processors.

Logic Analyzers for Real Time Trace of CPU Execution, Bus and I/O Traffic

The logic analyzer can also be configured to serve as the trace port collector. In this configuration, additional logic analysis cards can be used to monitor other buses within the system for time-correlated measurements of system activity. An integral emulation module can provide run control and register monitoring.